The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

***Ex parte*** KEVIN J. MCGRATH and MICHAEL T. CLARK



Appeal No. 2004-1122
Application No. 09/483,101

ON BRIEF

Before JERRY SMITH, GROSS, and BARRY, ***Administrative Patent Judges.***

GROSS, ***Administrative Patent Judge.***

***DECISION ON APPEAL***

This is a decision on appeal from the examiner's final rejection of claims 1 and 17. Claims 2 through 10 and 18 through 22 have been objected to as containing allowable subject matter but being dependent from a rejected base claim.

Appellants' invention relates to a processor having a segment register and a control register configured to support a first processing mode with an address size greater than 32 bits and an operand size of 32 or 64 bits and a second processing mode

with 32 bit and 16 bit processing. Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A processor comprising:

a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication, a second operating mode indication, and one or more bits identifying a segment described by said segment descriptor as a code segment;

a control register configured to store an enable indication, wherein said processor is configured to establish a default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication.

The prior art reference of record relied upon by the examiner in rejecting the appealed claims is:

James L. Turley, Advanced 80386 Programming Techniques, chapters 1, 2, 4, and 5 (McGraw-Hill 1988). (Turley)

Claims 1 and 17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Turley.

Reference is made to the Examiner's Answer (Paper No. 19, mailed October 22, 2003) for the examiner's complete reasoning in support of the rejection, and to appellants' Brief (Paper No. 18, filed September 2, 2003) and Reply Brief (Paper No. 20, filed November 21, 2003) for the appellants' arguments thereagainst.

***OPINION***

We have carefully considered the claims, the applied prior art reference, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the anticipation rejection of claims 1 and 17.

Claim 1 recites a processor that "is configured to establish a default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication." The examiner (Answer, page 5) considers Turley's segment privilege level bit (DPL) to be the first operating mode indication, Turley's granularity bit (G) to be the second operating mode indication, and Turley's protection enable bit (PE) to be the enable indication. The examiner explains (Answer, page 7)

> [W]hen the PE bit is not set, the segmentation described is disabled and, when the PE bit is set, the segmentation is enabled. Second, the DPL bit must match to allow access to the segment of memory. If access is not granted to the segment of memory, the segment cannot be accessed to set the address size. Finally, the G bit establishes the address size, since it is used as the default for determining the address size represented by the Limit field. The G bit indicates whether the address space size spans one megabyte (1MB) of space or up to four gigabytes (4GB) of space. Therefore, in order to establish a default address size, Protected mode must be enabled by the PE bit, the DPL bit must indicate that segment memory is accessible, and the G bit is accessed to establish the address size.

Appellants assert (Brief, page 4) that "Turley has no teaching or suggestion that the DPL is in any way related to default address size." According to appellants (Brief, page 4), "the privilege level may be used in determining if a memory access is granted or denied." However, appellants contend that such disclosure does not suggest that privilege level is a first operating mode that, together with a second operating mode indication and enable indication determine a default address size. Appellants also argue (Brief, page 4) that "the granularity bit, in conjunction with the limit field, defines the size of a segment." Appellants continue (Brief, page 5), "The G bit determines how to interpret the limit field, and defines the size of the segment. Addresses of the default address size (which is not determined by the G bit) would be used to address the segment, independent of the value of the G bit."

We agree with appellants. Assuming, ***arguendo***, that Turley's DPL and G bits are the first and second operating mode indications, Turley still fails to disclose that the processor is configured to establish a default address size responsive to DPL, G, and an enable indication. The examiner's explanation appears to equate address size with memory size. However, address size and memory size are not the same. As explained by appellants

***supra***, privilege level may be used to determine if a memory access is granted or not, but has no effect on default address size. See also Turley, page 84 and chapter 3. Similarly, the granularity bit (Turley, page 24) defines the size of a segment, not a default address size. Thus, since Turley fails to satisfy each and every limitation of claim 1, we cannot sustain the anticipation rejection of claim 1.

Claim 17 includes a limitation similar to that of claim 1. Specifically, claim 17 recites a step of "establishing a default address size in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor." As we explained ***supra***, even if we take Turley's DPL and G bits as the first and second operating mode indications, there is nothing in Turley that suggests establishing a default address size in response to an enable indication and the DPL and G bits. Therefore, Turley fails to disclose each and every limitation of claim 17, and we cannot sustain the anticipation rejection.

***CONCLUSION***

The decision of the examiner rejecting claims 1 and 17 under 35 U.S.C. § 102(b) is reversed.

***REVERSED***

JERRY SMITH )
Administrative Patent Judge )
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ANITA PELLMAN GROSS ) BOARD OF PATENT
Administrative Patent Judge ) APPEALS
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) INTERFERENCES
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LANCE LEONARD BARRY )
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